A METHOD TO ENHANCE INDUCTOR Q FACTOR BY FORMING AIR GAPS BELOW INDUCTORS

FIELD OF THE INVENTION

The present invention relates generally to fabrication of semiconductor devices, and more specifically to methods of enhancing the performance of inductors.

BACKGROUND OF THE INVENTION

The quality factor (Q factor) is affected by capacitance loss due to coupling to underlying metals and substrate loss due to eddy current.

U.S. Patent No. 6,180,995 B1 to Herbert describes an air gap under a field oxide under inductors.

U.S. Patent No. 6,307,247 B1 to Davies describes an inductor process with low-k layers.

U.S. Patent No. 6,287,979 B1 to Zhou et al. describes an air gap process between conductive lines.

U.S. Patent No. 4,634,494 to Taji et al. describes a process to selectively etch a doped oxide layer.

U.S. Patent No. 5,742,091 to Hébert describes a semiconductor device within which parasitic capacitances are minimized and a method of fabricating same.

U.S. Patent No. 6,303,423 to Lin describes a method for forming high performance system-on-chip using post passivation process.

SUMMARY OF THE INVENTION

Accordingly, it is an object of the present invention to provide improved methods of fabricating inductor devices with reduced capacitance loss.

Other objects will appear hereinafter.

It has now been discovered that the above and other objects of the present invention may be accomplished in the following manner. Specifically, a structure having a first oxide layer formed thereover is provided. A lower low-k dielectric layer is formed over the first oxide layer. A second oxide layer is formed over the lower low-k dielectric layer. The second oxide layer is patterned to form at least one hole there through exposing a portion of the lower low-k dielectric layer. Etching through the exposed portion of the lower low-k dielectric layer and into the lower low-k dielectric layer to from at least one respective air gap within the etched lower low-k dielectric layer. An upper low-k dielectric layer is formed over the patterned second oxide layer. At least one inductor is formed within the upper low-k dielectric layer and over the at least one air gap whereby the performance of the inductor is enhanced.

BRIEF DESCRIPTION OF THE DRAWINGS

The features and advantages of the present invention will be more clearly understood from the following description taken in conjunction with the accompanying drawings in which like reference numerals designate similar or corresponding elements, regions and portions and in which:

Figs. 1 to 5 schematically illustrate in cross-sectional representation a preferred embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Initial Structure

Fig. 1 illustrates a cross-sectional view of a structure 10 that is preferably a silicon (Si), germanium (Ge), gallium arsenide (GaAs), or any compounded semiconductor or polymeric material substrate, is more preferably a silicon substrate and is understood to possibly include a semiconductor wafer or substrate, active and passive devices formed within the wafer, conductive layers and dielectric layers (e.g., inter-poly oxide (IPO), intermetal dielectric (IMD), etc.) formed over the wafer surface. The term "semiconductor structure" is meant to include devices formed within a semiconductor wafer and the layers overlying the wafer. Structure 10 may include several levels of metal interconnects with an uppermost exposed metal interconnect 11.

A first oxide layer 12 is formed over structure 10 to a thickness of preferably from about 1000 Å to 5μm and may be from about 3000 to 6000Å. First oxide layer 10 is preferably comprised of silicon oxide (SiO_2), doped silicon oxide, BPSG, FSG, silicon carbide (SiC), Coral™, Black Diamond™, SiN or TEOS and is more preferably silicon oxide (SiO_2).

A via opening 17 is formed within first oxide layer 12 and a planarized metal plug 18 is formed within via opening 17.

A low-k dielectric layer 14 is formed over first oxide layer 12 and metal plug 18 to a thickness of preferably from about 1000 to 10,000Å and more

preferably from about 2000 to 6000Å. Low-k dielectric layer 14 is preferably comprised of silicon oxide (SiO_2), boron-doped silicon oxide, phosphorous-doped silicon oxide, BPSG, FSG, SiN or carbon doped silicon oxide such as Coral™ or Black Diamond™ and is more preferably carbon-doped silicon oxide.

A trench opening 19 is formed within low-k dielectric layer 14 and a planarized metal structure 20 is formed within trench opening 19. Metal plug 18 and metal structure 20 comprise a dual damascene structure 22 and is preferably comprised of copper (Cu), tungsten (W), aluminum (Al), tantalum (Ta) or tantalum nitride (TaN) and is more preferably copper.

A second oxide layer 16 is formed over low-k dielectric layer 14 and metal structure 20 to a thickness of preferably from about 1000 to 10,000Å and more preferably from about 4000 to 8000Å. Second oxide layer 16 is preferably comprised of silicon oxide (SiO_2), doped silicon oxide, BPSG, FSG, Coral™, Black Diamond™, SiN or silicon carbide (SiC) and is more preferably silicon oxide (SiO_2).

Formation of Holes 24, 26

As shown in Fig. 2, one or more holes 24, 26 are formed through second oxide layer 16 preferably using a dry etch, a wet etch or a combination wet/dry etch and more preferably a dry etch. Holes 24, 26 have a width of preferably from about 1.0 to 10.0μm and more preferably from about 2.0 to 6.0μm and expose portions 25, 27 of low-k dielectric layer 14.

Holes 24, 26 may be formed by, for example, forming a patterned masking layer (not shown) over the second oxide layer 16 and then using the patterned masking layer as a mask to etch holes 24, 26. The patterned masking layer may be comprised of, for example, a photoresist layer.

Formation of Lower Air Gaps 28, 30

As shown in Fig. 3, a solvent etch is used to etch low-k dielectric layer 14 through the exposed portions 25, 27 of low-k dielectric layer 14 to form respective air gaps 28, 39 within etched low-k dielectric layer 14'. The solvent etch is selected to have a second/first oxide layer 16/12 : low-k dielectric layer 14 etch selectivity of preferably about 1 to 10 and more preferably from about 1:50 to 1:100 so that only low-k dielectric layer 14 is appreciably affected by the solvent etch. This obviates the need to have a patterned mask layer formed over etched second oxide layer 16' before the solvent etching of low-k dielectric layer 14.

Air gaps 28, 39 have respective diameters 31, 33 of preferably from about 100.0 to 500.0μm and more preferably from about 200.0 to 400.0μm.

Formation of Upper Low-k Dielectric Layer 32

As shown in Fig. 4, an upper low-k dielectric layer 32 is formed over etched second oxide layer 16, sealing holes 24, 26 and thus air gaps 28, 30. Upper low-k dielectric layer 32 has a thickness of preferably from about 0.1 to 10.0μm and more preferably from about 2.0. to 5.0μm. Upper low-k dielectric layer 32 is

preferably comprised of silicon oxide, TEOS, SiC, SiN, FSG, BPSG or carbon-doped silicon oxide such as Coral™ or Black Diamond™ and is more preferably FSG.

Formation of Inductor 34

As shown in Fig. 5, an inductor 34 is formed within upper low-k dielectric layer 32 over air gap(s) 28, 30. The presence of air gaps 28, 30 decreases the dielectric constant (k) of the material underlying the inductor 34 and therefore decreases: (1) the capacitance loss of the inductor 34 due to coupling to underlying metal layers, i.e., e.g. dual damascene structure 22 as illustrated in the Figures; and (2) the substrate loss due to eddy current. This enhances the inductor 34.

Such eddy currents are closed loops of induced current circulating in planes perpendicular to the magnetic flux. They normally travel parallel to the coil's winding and the flow is limited to the area of the inducing magnetic filed. Eddy currents concentrate near the surface adjacent to a coil and their strength decreases with the distance from the coil as shown in the image. Eddy current density decreased exponentially with depth.

It is noted that only one, or more than two air gaps 28, 30 may be formed within low-k dielectric layer 14 so that any inductors 34 formed within upper low-k dielectric layer 32 are formed over the air gaps 28, 30 so formed.

It is also noted that the air-gap(s) 28, 30 and the inductor 34 can be at any relative layers. For example, the 'first oxide layer 12' may be from M1 through

M6 with the air gap(s) 28, 30 and the inductor 34 at M7 and M8, respectively. Thus, a thick 'first oxide layer 12' is given.

Advantages of the Invention

The advantages of one or more embodiments of the present invention include:

1) the reduction of coupling with the substrate thereby enhancing the quality factor of the metal inductors formed in accordance with the present invention; and
2) the method of the present invention can be integrated with any back-end-of line (BEOL) technologies, regardless of whether Cu or Al is implemented.

While particular embodiments of the present invention have been illustrated and described, it is not intended to limit the invention, except as defined by the following claims.